REMARKS

The Examiner stated the communication of April 14th, 2006 was not a final rejection. Applicants note that box 2A was checked and this lead to Applicants believing the action was final.

The Examiner rejected claims 1-13 under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The Examiner rejected claims 1-20 and 30 under 35 U.S.C. 102(e) as being anticipated by Evans et al. (U.S. Patent 6,279,146).

The Examiner rejected claims 21-29 under 35 U.S.C. 103 as being unpatentable over Evans in view of Dutta et al. "Viper."

Applicants respectfully traverse the §101, §102 and §103 rejections with the following arguments.

35 USC § 101 Rejections

The Examiner rejected claims 1-13 under 35 U.S.C. 101 "because the claimed invention is directed to non-statutory subject matter." The Examiner further stated "The claims recite a system and method that appears to be code. It should be noted that code (i.e. a computer software program) does not do anything per se. Instead it is the code stored on a computer that when executed, instructs the computer to perform various functions." The Examiner then gave a generic example of a proper computer product claim

In response, applicants have canceled independent claims 1 and 8 and supplied a new claim 31 written in proper computer system form. Applicants believe claim 31 meets the requirements of 35 U.S.C. 101.

35 USC § 102 Rejections

Applicants respectfully point out, Applicants are teaching testing a computer simulation model of and integrated circuit chip derived from an integrated circuit chip design (which itself is a software description of a physical integrated circuit) with test devices (e.g. an external memory mapped test device) that are also computer simulations. Other than the computer running the test operating system sending instructions to the computer simulated model and the computed simulated test devices there is no hardware in Applicants invention.

Evans et al. is teaching testing a physical integrated circuit design modeled in a physical field programmable gate array (FPGA) (see FIG. 6, steps 310-316). While software is used by Evans et al. in the verification system of Evans as indicated by the Examiner, Applicants respectfully point out that the software is used to program the FPGA to represent the integrated circuit chip, run the tests and otherwise perform verification of the integrated circuit design. The Examiner also indicated that Evans et al. teaches virtual bus wrappers. Applicants point out that Evans states in col. 11, line 11 "Some bys wrappers 140 must serve as virtual bus wrappers" but bus wrapper 140 is implemented as a FPGA (See FIG. 4) so the virtual bus wrappers are also physical models of the bus design of the integrated circuit chip." Therefore, it is a hardware model (i. e., an FPGA model) of the integrated circuit chip that is being tested and verified by Evans et al. not a computer simulation that only exists on a computer memory.

As per claim 31, based on the discussion *supra*, clearly Evans is teaching a hardware model of the integrated circuit design and not "a computer simulation model of said integrated circuit design" as Applicants claim 31 requires. Therefore Applicants maintain claim 31 is not unpatentable over Evans et al. and is condition for allowance. Since claims 2, 3, 5, 7 and 21-23,

23, 33 depend from claim 31, Applicants maintain claims 2, 3, 5, 7, 21-23, 32 and 33 are likewise in condition for allowance.

As per claim 14, the Examiner has indicated that Evans et al. col. 10, line 60 to col. 11, line 26 (which describes FIG. 5) and FIGs. 2 and 5 teach the following clauses from Applicants claim 14:

(1) "providing an I/O controller connected to one or more I/O cores, said I/O cores part of said integrated circuit design;"

(2) "providing an external memory mapped test device having a switch for selectively connecting one or more of said I/O cores to corresponding I/O driver models;"

(3) "distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models;" and

(4) "providing an additional external memory mapped test device module directly connected to one or more additional I/O driver models, each additional I/O driver model directly connected to an additional I/O core, each additional I/O core part of said integrated circuit design."

Applicants respectfully point out that Evans et al. FIG. 2 illustrates a block diagram of a verification engine with FPGA 72 configured as a FPGA model of the integrated circuit 10 of FIG. 1 and FPGA 66 configured with the only I/O driver (UART port) connected to a simulation host computer 118, FIG. 5 illustrates the details of bus wrappers 140 (which are FPGAs) of cards 120 of FIG. 4, and col. 10, line 60 to col. 11 line 26 just describes FIG. 5. Applicants maintain

that Evans et al. col. 10, line 60 to col. 11, line 26 and FIGs. 2 and 5 does not teach clauses (1), (2), (3) or (4) from Applicants claim 14 as the Examiner alleges.

Applicants cite *infra*, examples of deficiencies in the teaching of Evans et al. relative to Applicants claim 14.

Applicants find no teaching relative to clauses (1), (2), (3) and (4) if claim 14 cited *supra* of I/O controllers, I/O cores, I/O driver models, additional I/O driver models or additional I/O cores and no detailed teaching relative to clauses (2) and (4) of claim 14 cited *supra* of an external memory mapped devices and can not identify any structures taught in Evan et al that are their equivalents.

Further, Applicants see no teaching in Evan et al. of element connections such as (A) "an I/O core connected to one or more I/O cores," (B) "an external memory mapped test device having a switch for selectively connecting one or more of said I/O cores to corresponding I/O driver models," (C) "distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models," (D) "providing an additional external memory mapped test device module directly connected to one or more additional I/O driver models," and (E) "each additional I/O driver model directly connected to an additional I/O core, each additional I/O core part of said integrated circuit design" as Applicants claim 14 requires.

Therefore, Applicants maintain claim 14 is not unpatentable over Evans et al. and is condition for allowance.

As per claim 15, Applicants maintain the arguments present *supra*, relative to claim 14 are applicable to claim 15.

Further, since Evans et al. clearly teaches the model of the integrated circuit being implemented in FPGA (hardware), Evans et al. can not be teaching "wherein said simulated I/O cores, said simulated general purpose I/O core and said simulated I/O controller comprise a computer model of said integrated circuit design" as Applicants claim 15 requires.

Therefore claim 14 is also in condition for allowance. Since claims 16-20 and 27-29 depend from claim 15, Applicants maintain claims 16-20 and 27-29 are likewise in condition for allowance.

35 USC § 103 Rejections

First, as to claims 21-23 and 27-29, Applicants have argued *supra* in response to the Examiners § 102(e) rejection of claims 1, and 15 that new claims 31 and amended claim 15 are allowable, since claims 21-23 depend from claim 31, claims 27-29 depend from claim 15, Applicants respectfully maintain that claims 21-23 and 27-29 are not unpatentable over Evans et al. in view of Dutta et al. and are in condition for allowance.

Second, as to claims 21-23 and 27-29, Applicant maintain the rejections are improper because there is no suggestion in the prior art to combine the references as required by *Karsten Mfg. Corp. v. Cleveland Gulf Co.*, 242 F.3d 1376, 1385, 58 U.S.P,Q.2d 1286, 1293 (Fed. Cir. 2001) which states " In holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in the way that would produce the claimed invention." The alleged motivation does originate from prior art but has been supplied by the Examiner. Further, the Examiner has not offered any evidence that the motivation was "in the knowledge generally available to one of ordinary skill in the art" and has impermissibly shifted the burden of proof to Applicants. Therefore, the Examiner has not established his prima facie case of obviousness.

Applicants point Dutta et al. merely includes a 1394 core in the "Viper" circuit while Evan et al. teaches FPGA core models. Thus neither Dutta et al. or Evans et al. teach or suggest a computer "*simulated* 1394 I/O" as Applicants claim 21 requires.

Applicants remind the Examiner that claims 15 and 31 from which claims 21 and 23 and 27-29 depend respectively require that simulated cores of claims 21, 23 and 27-39 be computer simulations.

Applicants point Dutta et al. merely includes a DMA core in the "Viper" circuit while Evan et al. teaches DMA core models. Thus neither Dutta et al. or Evans et al. teach or suggest a computer "*simulated* direct memory access core as Applicants amended claim 23 requires.

As to claim 27, Applicants point Dutta et al. merely includes a UART core in the "Viper" circuit Evan et al. teaches FPGA core models. Neither Dutta et al. or Evans et al. teach or suggest a computer "*simulated* asynchronous receiver transmitter core" as Applicants amended claim 27 requires.

As to claim 28, Applicants point Dutta et al. merely includes a UART core in the "Viper" circuit Evan et al. teaches FPGA core models. Neither Dutta et al. or Evans et al. teach or suggest a computer "*simulated* direct memory access core" as Applicants amended claim 28 requires.

As to claim 29, Applicants point Dutta et al. merely includes a UART core in the "Viper" circuit Evan et al. teaches FPGA core models. Neither Dutta et al. or Evans et al. teach or suggest a computer "*simulated* direct memory access core" as Applicants amended claim 28 requires.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR:
Devins et al.

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